Peter Miller

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Summary

Electrical Engineer with a focus on digital and computer engineering. Experience with CPU architecture design, digital logic design and layout, RTL design, embedded system design and system level testing. Looking for co-op or full time position.

Work Experience

RIT Center for Detectors – Rochester, NY Student Software Engineer August 2018 – May 2019

- Designed Photonic Integrated Circuit (PIC) stand-in for testing of PIC verification tools
- Created PCB layout for PIC stand-in
- Constructed PIC stand in including many SMD components

Advanced Micro Devices – Austin, TX Co-op Engineer January 2018 – May 2018

- Helped set up System Level Testing (SLT) for 7nm Radeon Instinct and Radeon VII GPUs
- Began thermal evaluations for Radeon Instinct and Radeon VII GPUs
- Improved and streamlined existing SLT tools
- Created tool to make SLT & ATE testing procedures easier to set up and understand
- Set up open source iPXE as a seamless replacement for PXE to solve upcoming compatibility issues

Teledyne Scientific Co. – Durham, NC Technical Intern March 2017 – August 2017

- Developed, improved and overhauled MATLAB scripts for bulk image processing
- Trained and help supervise another intern with using these scripts
- Ran experiments to test and refine software
- Worked to compile and set up a custom kernel for an Nvidia TX1 Jetson development board
- Prepared slides for review by government

Teledyne Scientific Co. – Durham, NC Software Intern July 2016 – August 2016

- Developed and improved MATLAB scripts for bulk image processing

Education

Rochester Institute of Technology – Rochester, NY 2014 – 2019
BS Electrical Engineering with Computer Engineering Option

Skills

General: Debugging, problem solving, design & verification, layout
Hardware: Intel/Altera FPGA, TI MSP430, Arduino, Raspberry Pi, Nvidia TX1
Languages: Verilog, VHDL, Assembly, C/C++, Java, MATLAB, Unix Shell, Javascript, HTML, CSS, Batari Basic
Software: Linux, Cadence Virtuoso, Intel Quartus

Projects

OLLAR & PAM_RISC521 Processors

- RISC processors developed in Verilog for the Altera Cyclone IV & V FPGAs
- PAM_RISC521 was developed for RIT's EEEE521 Design of Computer Systems course
- OLLAR (Open-source License Logic & Arithmetic RISC) is being developed as an open-source RISC processor with goals of being easy to modify and understand
- OLLAR will be provided with documentation on its detailed workings to enhance its potential as a learning aid
- Both processors can implement multiple cores and a four-stage pipeline
- PAM_RISC521 Implements a cache

Satellite Tracking Automated Receiver (STAR)

- Multidisciplinary Senior Design project designed to track satellite passes and record their radio transmissions
- Eliminates need for manual tracking at odd times of day or in poor weather
- Designed core of control firmware including a text-based interface for receiving commands

Who's Really In Charge?

- Created a homebrew puzzle game for the Atari 2600 that leverages limitations and specific hardware aspects of the 2600 as key components of the puzzles
- Written in Batari Basic, runs in Stella emulator and on real hardware using a Harmony Cartridge
- Booklet was written by partner which gives important information, in the form of a story, to the user for gameplay of each puzzle, with each puzzle directing the user to a specific page in the booklet

Groups

Boy Scouts of America	2006 – 2014
• Order of the Arrow	2009 – Present
• Eagle Scout	2014
Cum Laude Society	2014 – Present
RIT Linux Users Group	2014 – 2019
National Society of Leadership & Success	2016 – Present
Order of the Engineer	2019 – Present